CEC IIe

SINGLE BOARD COMPUTER

INSTRUCTION MANUAL

1985 (Rev.A)

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CEC IIe OPERATING INSTRUCTION

I. Introduction.

CEC IIe is an 8 bit personal computer using a 6502 CPU with 64K ROM SLOT (J21), one 60 pin auxiliary slot for 80 Column Text Card, and seven I/O slots for General Purpose peripheral cards to extend the computer's capability.

Keyboard interface is provided with a 16 pin DIP socket; each pin name is described in chapter III.Game I/O is also built into the board with a 16 pin DIP socket (J15) and 9 pin D type connector (J8) to connect with the outside world. Speaker, Casette and Video interfaces are provided.

There are two switches on CEC IIe that will activate two special functions:

A. Forced cold start.

Remove JP3, hold down the CONTROL key and then press and release the RESET key; you can force a cold start instead of turning the power off and on. If you don't use the cold start function, JP3 must be in place.

B. Automatic self-test.

Remove JP4, hold down the CONTROL key; then press and release the RESET. CEC IIe will start running the built-in self-test. The self-test takes several seconds to run. While it is running, the display changes from black to white and back twice. If the test finishes normally, the CEC IIe displays a message "KERNEL OK" and waits for you to request a normal reset. After doing automatic self-test;remember to insert the JP4 jumper to do the normal reset.

II. Installation.

1. Turn off the system unit power.
2. Connect the keyboard to J17.
3. Connect the Video cable from J11 to Video monitor.
4. Insert the ROM CARD into J21, component side faceing the righthand side, components facing away from the power connectors.
5. Insert the 80 column text card into J0 if you want 80 column display.
6. Insert any peripheral card into an expansion slot if desired.
7. Connect power cable to power connector.
8. Turn on the system unit power.
9. Remove JP4 shorting plug and press CONTROL RESET KEY. The automatic self-test will start. If there are no errors, the monitor will display "KERNEL OK".

III. CONNECTOR SPECIFICATION:

1. The Auxiliary Slot (J0) Pin Assignment

Pin no.	Name	Description
1	3.58M	3.58MHz video color reference signal. This line drives 2 LS TTL loads.
2	VIDTM	Clocks the video dot out of the parallel-to-serial shift register. This line drives 2 LS TTL loads.
3	SYNC*	Video horizontal and vertical sync signal. This line drives 2 LS TTL loads.
4	PRAS*	Mutiplexed RAM row-address strobe. This line drives 2 LS TTL loads.
5	VC	Third low-order vertical-counter bit. This line drives 2 LS TTL loads.
6	C07X*	Hand-control reset signal. This line drives 2 LS TTL loads.
7	WNDW*	Video non-blank window. This line drives 2 LS TTL loads.
8	SEGA	First lower vertical counter bit. This line drives 2 LS TTL loads.
9,46,14, 13,48,49, 10,51	RA7-RA0	Multiplexed Ram-address bus. This line drives 2 LS TTL loads.
11,12	ROMEN1, ROMEN2	Enable signals for the ROMs on the ROM card.
15,18,19, 22,38,41, 42,45	VID0-VID7	Video data bus. This three-state bus carries video data to the character generater.
16,17,20, 21,39,40, 43,44	MD7-MD0	Internal data bus. This line drives 2 LS TTL loads.
23	0	6502 clock phase 0. This line drives 2 LS TTL loads.

Pin no.	Name	Description
24	CLRGAT*	Color-burst gating signal. This drives 2 LS TTL loads.
25	80VID*	Enables 80-column display timing. This line drives 2 LS TTL loads.
26	EN80*	Enable for auxiliary RAM. This line drives 2 LS TTL loads.
27	ALTVID*	Alternative video output to the video summing amplifier.
28	SEROUT*	Video serial output from parallel-to-serial shift register.
29	ENVID*	Normally low; driving this line high disables the character generator such that the video dots from the shift register are all high (white). and alternative video can be sent out via ALTVID'. This line has a 1000 ohm pulldown resistor to ground.
30	+5V	+5V power supply.
31	GND	System common ground.
32	14M	14.3MHz master clock signal. This line drives 2 LS TTL loads.
33	PCAS*	Multiplexed column-address strobe. This line drives 2 LS TTL loads.
34	LDPS*	Strobe to video parallel-to-serial shift register. This signal goes low to load the contents of the video data bus into the shift register. This line drives 2 LS TTL loads.
35	R/W 80	Read/write signal for RAM on the 80-column text card. This line drives 2 LS TTL loads.
36	1	6502 clock phase 1. This line drives 2 LS TTL loads.

Pin no.	Name	Description
37	CASEN*	Column-address enable. This signal is disabled (held high) during accesses to memory on the auxiliary card. This line drives 2 LS TTL loads.
47	HO	Low-order horizontal byte counter. This line drives 2 LS TTL loads.
50	AN3	Output of annunciator 3. This line drives 2 LS TTL loads.
52	R/W*	6502 read/write signal. This line drives 2 LS TTL loads.
53	Q3	2MHz asymmetrical clock. This line drives 2 LS TTL loads.
54	SEGB	Second low-order vertical-counter bit. This line drives 2 LS TTL loads.
55	ENFIRM	Normally high; pulling this line low disables ROM1 and ROM2 on the ROM CARD.
56,57	RA9*,RA10*	Character-generator control signals from the IOU . This line drives 2 LS TTL loads.
58	GR	Graphics-mode enable signal. This line can drive 2 LS TTL loads.
59	7M	7MHz timing signal. This line drives 2 LS TTL loads.
60	ENTMG*	Normally low; pulling this line high disables the master timing from the PAL.

Pin no.	Name	Description
25	+5V	+5 Volt power supply.
26	GND	System common ground.
27	DMA IN	DMA priority daisy-chain input. Usually connected to pin 24 (DMA OUT).
28	INT IN	Interrupt priority daisy-chain input. Usually connected to pin 23 (INT IN).
29	NMI*	Non-maskable interrupt to 6502. Pulling this line low starts an interrupt cycle.
30	IRQ*	Interrupt request to 6502. Pulling this line low starts an interrupt cycle only if the interrupt-disable (I) flag in the 6502 is not set.
31	RES*	Pulling this line low initiates a reset routine.
32	INH*	Pulling this line low during 1 inhibits (disables) the memory on the main circuit board.
33	-12V	-12V power supply.
34	-5V	-5V power supply.
35	3.58M	3.58MHz color reference signal, on slot 7 only. This line drives 2 LS TTL loads.
36	7M	System 7MHz clock. This line drives 2 LS TTL loads.
37	Q3	System 2MHz asymmetric clock. This line drives 2 LS TTL loads.
38	1	6502 phase 1 clock. This line drives 2 LS TTL loads.
39	uPSYNC	The 6502 signals an operand fetch by driving this line high during the first read cycle of each instruction.

Pin no	Name	Description
40	0	6502 phase 0 clock. This line drives 2 LS TTL loads.
41	DEV1*	Normally high; goes low during 0 when the 6502 addresses location $Conx, where n is the slot number plus 8. This line drives 10 LS TTL loads.
42-49	D0-D7	Three-state buffered bi-directional data bus. Data becomes valid during 0 high and remains valid until 0 goes low. Each data line can drive one LS TTL loads.
50	+12V	+12 volt power supply.

3. Game I/O Connector Signals.

J15 Pin no.	J8 Pin no.	Signal Name	Description
1	2	+5V	+5V power supply.
2	7	SW/OAPC	Switch input, a standard 74 LS input.
3	1	SW1/CAPL	Switch input, a standard 74 LS input.
4	6	SW2	Switch input, a standard 74 LS input.
5	-	STB	Strobe output. This line goes low during 0 of a read or write instruction to location $C040.
6,10, 7,11	5,8, 4,9	PDL0-PDL3	Hand control inputs. Each of these should be connected to a 150K-ohm variable resistor connected to +5V
8	3	GND	System ground.

J15 Pin no.	J8 Pin no.	Signal Name	Description
15,14, 13,12	-	AN0-AN3	Annuciators. These lines are standard 74 LS TTL outputs.
9,16	-	N.C.	Nothing is connected to these pins.

4. Cassette I/O (J9,J10).

J9 Phone jack is used as an input from the cassette recorder.

J10 Phone jack is used as an output to the cassette recorder.

The signal specification for cassette I/O are:

Input: 1 volt (nominal) from recorder Earphone or Monitor output. Input impedance is 12K ohms.
Output: 25 millivolts to recoder Microphone input. Output impedance is 100 ohms.

5. The Speaker (J18).

Pin no.	Name	Description
1	SPKR	Speaker signal. This line will deliver about 0.5 watts into an 8-ohm speaker.
2	+5V	+5V power supply.

6. The Keyboard Connector (J17).

Pin no.	Name	Description
1	+5V	+5V power supply.
2	KSTRB	Strobe output from keyboard. This line should be given a pulse at least 10us long each time a key is pressed on the keyboard. THe strobe can be of either polarity.
3	RESET	6502's reset line. Normally high; this line should be pulled low to restart the computer.
4,9	NC	No connection.
8	GND	System common ground.
12,13,10, 11,6,5,7	DATA0-DATA6	Seven bit ASCII Keyboard data input.
14	SW0/OAPL	Switch input, a standard 74 LS TTL input, normally low.
15	-12V	-12 volt power supply.
16	SW1/CAPL	Switch input, a standard 74 LS TTL input, normally low.

7. Video Output Signals (J11,J13).

The video signal is an NTSC-compatible composite-video signal that can be displayed on a standard video monitor. This signal is available in two places; J11 (RCA JACK) and J13 (Molex-type pins) on J11. The sleeve of this jack is connected to ground and the tip is connected to the video signal on J13. The pin assignment is as follows:

Pin no.	Name	Description
1	GROUND	System common ground.
2	VIDEO	NTSC-compatible positive composite video. White level is about 2.0 volts, black level is about 0.75 volts, and sync level is 0 volts.
3	-5V	-5V power supply.
4	+12v	+12V power supply.

8. Power Connector (J14, J20).

J20 pin assignment:

Pin no.	Name	Description
1	Ground	Common electrical ground.
2	+12V	+12V from power supply.
3	-5V	-5V from power supply.
4	-12V	-12V from power supply.
5	+5V	+5V from power supply.
6	+5V	+5V from power supply.

J14 pin assignment:

Pin no.	Name	Description
1	Ground	Common electrical ground.
2	Ground	Common electrical ground.
3	+5V	+5V form power supply.
4	+12V	+12V from power supply.
5	-12V	-12V from power supply.
6	-5V	-5V from power supply.

9. ROM Slot.

ROM slot is a 16K ROM expansion card to install the dedicated operating program for the CEC IIe single board computers.

Pin assignment as follows:

Pin no.	Name	Description
1,15-24, 37-48,50	N.C.	No connection.
2-14	A0-A12	Three state address lines from 6502.
25	+5V	+5V power supply.
26	GND	System ground.
27-34	MD7-MD0	Internal data bus.
35,36	ROMEN1*, ROMEN2*	Enable signals for the ROMs.
49	ROMOE*	Enable signals for the ROMs on the ROM card.

IV. POWER REQUIREMENT.

To operate the CEC IIe plus a full complement of peripheral cards, including disk controller cards and communications interfaces, we suggest the basic power specification as follows:

Maximum power consumption: 60W continuous
80W intermittent

Voltages and Maximum current:

a. +5V (±3%): 2.5A

b. +12V (±6%): 1.5A continuous
2.5A intermittent

c. -5V (±10%): 250 MA

d. -12V (±10%): 250 MA

V. TROUBLE SHOOTING.

During use of the CEC IIe single board computer should any trouble occur, do the following:

1. Make sure JP3 and JP4 short plugs are in position when the CEC IIe is in normal use.

2. Remove JP4 and press CONTROL RESET on keyboard to start self-test. If test fails, contact the dealer for repair.

3. When a color monitor is used but color is not correct,try to adjust the color trimmer VC1 and VC2 to get the right color. If there is no color, adjust VC1 first, then VC2.

4. If there is any trouble you can not fix, contact your dealer.

VI. TECHNICAL INFORMATION.

1. The PAL Circuit.

A Programmed Array Logic device, type PAL 16R8,generates several timing and control signals in the CEC IIe. These signals are listed as follows:

The PAL pinout:

14M	1	20	+5V
H0	2	19	VID7M
80VID*	3	18	PRAS*
VID7	4	17	0
3.58M	5	16	LDPS*
CASEN*	6	15	Q3
GR	7	14	O1
7M	8	13	N.C.
SEGB	9	12	PCAS
GND	10	11	ENTMG*

Pin no.	Name	Description
1	14M	14.31818 MHz master timing signal.
2	HO	Horizontal videos timing signal.
3	80VID*	Enable 80-column display mode.
4	VID7	Video data bit 7.
5	3.58M	3.579545 MHz timing signal.
6	CASEN*	RAM enable.
7	GR	Video display graphics-mode enable.
8	7M	7.15909 MHz timing signal.
9	SEGB	Video timing signal.
10	GND	Power and signal common.
11	ENTMG*	Enable master timing.
12	PCAS*	RAM column-address strobe.
13	N.C.	(This pin is not used.)
14	1	Phase 1 system clock.
15	Q3	Intermediate timing and strobe signal.
16	LDPS*	Video shift-register enable.
17	0	Phase 0 system clock.
18	PRAS*	RAM Row-address strobe.
19	VID7M	Video dot clock, 7 or 14 MHz.
20	+5V	Power.

2. The Input/Output Unit 65301

65301 is designed with CMOS techonology; it implements the following soft switches:

Page 2 display (PAGE2), Hi-res mode (HIRES), Text mode (TEXT), Mixed mode (MIXED), 80-column display (80 col), character-set select (ALTCHARSET) Any-key-down, Annunciators, Vertical blanking (VBL). The IOU generates the multiplexed address for the 64K dynamic RAMs used in the CEC IIe for the data transfers required for display and memory refresh during clock phase 1.

The 65301 pinout:

VC	1	40	SEG B
60/50	2	39	SEG A
WNDW*	3	38	GR
SYNC*	4	37	VID 6
CLRGAT*	5	36	VID 7
HO	6	35	RA10
RA0	7	34	RA9
RA1	8	33	AKD
RA2	9	32	KSTRB
RA3	10	31	VDD
GND	11	30	80 VID
RA4	12	29	AN0
RA5	13	28	AN1
RA6	14	27	AN2
RA7	15	26	AN3
0	16	25	RESET*
Q3	17	24	MD7
PRAS*	18	23	R/W
A6	19	22	CASS0
COXX*	20	21	SPKR

Pin no.	Name	Description
1	VC	Display vertical counter bit.
2	60/50	60Hz or 50 Hz.
3	WNDW*	Display blanking signal.
4	SYNC*	Display synchronization signal.
5	CLRGAT*	Color-burst gate.

Pin no.	Name	Description
6	HO	Display horizontal timing.
7-10	RA0-RA3	Multiplexed RAM address (phase 0).
11	GND	Signal common.
12-15	RA4-RA7	Multiplexed RAM address (phase 0).
16	0	Master clock phase 0.
17	Q3	Intermediate timing signal.
18	PRAS*	Row-address strobe (phase 0).
19	A6	Address bit 6 from 6502.
20	COXX*	I/O address enable.
21	SPKR	Speaker output signal.
22	CASS0	Cassette output signal.
23	R/W	6502 Read-Write control signal.
24	MD7	Internal flag to data bus
25	RESET*	Power on and reset output.
26-29	AN3-AN0	Annunciator output.
30	80VID*	80-column video enable.
31	VDD	+5V System power.
32	KSTRB	Keyboard strobe signal.
33	AKD	Any-key-down signal.
34-35	RA9,RA10	Video display control bits.
36-37	VID7,VID6	Video data bits.
38	GR	Graphics mode enable.
39,40	SEGA,SEGB	Display vertical counter bits.

3. The Memory Management Unit 65371

65371 is designed with CMOS technology, implements the following soft-switches:

Page 2 display (PAGE2), Hi-res mode (HIRES), store to 80-column card (80 STORE), select bank 2, enable bank-switched RAM, read auxiliary memory (RAMWRT), auxiliary stack and zero page (ALTZP), slot ROM for connector #3 (SLOTC3ROM), slot ROM in I/O space (SLOTCXROM). The 65371 generates multiplexed address for memory reading and writing by the 6502 CPU.

The 65371 pinouts:

CXXX	1	40	CASEN*
R/W245*	2	39	INH*
ROMEN1*	3	38	R/W*
EN80*	4	37	ROMEN2*
0	5	36	KBD*
PRAS*	6	35	DMA*
Q3	7	34	A15
RA7	8	33	A14
RA6	9	32	A13
RA5	10	31	A12
GND	11	30	VDD
RA4	12	29	A11
RA3	13	28	A10
RA2	14	27	A9
RA1	15	26	A8
MD7	17	24	A6
A0	18	23	A5
A1	19	22	A4
A2	20	21	A3

Pin no.	Name	Description
1	CXXX	Enables peripheral-card memory.
2	R/W245*	Control data bus buffer.
3	ROMEN1*	Enables ROM #1.
4	EN80*	Enables auxiliary RAM.
5	0	Clock phase 0.
6	PRAS*	Memory row-address strobe.
7	Q3	Timing signal.
8-10	RA7-RA5	Multiplexed address output.
11	GND	Signal common.
12-16	RA4-RA0	Multiplexed address output.
17	MD7	Data bus bit.
18-29	A0-A11	6502 address output.
30	VDD	+5V system power.
31-34	A12-A15	6502 address output.
35	DMA*	Controls data bus for DMA transfer.
36	KBD*	Enables keyboard data bits.
37	ROMEN2*	Enables ROM #2.
38	R/W*	6502 read write control signal.
39	INH*	Inhibits main memory.
40	CASEN*	Enables RAM.

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CEC IIe MOTHER BOARD PARTS LIST:

PART #	ITEM	QTY
MB-PCB	MOTHER BOARD - P.C.B.	1
LS-004	I.C. 74LS04 (U25)	1
LS-010	I.C. 74LS10 (U8)	1
LS-125	I.C. 74LS125 (U12)	1
LS-138	I.C. 74LS138 (U16)	1
LS-166	I.C. 74LS166 (U7)	1
LS-244	I.C. 74LS244 (U19,20,27)	3
LS-245	I.C. 74LS245 (U2)	1
LS-251	I.C. 74LS251 (U26)	1
LS-374	I.C. 74LS374 (U6)	1
OS-002	I.C. 74S02 (U21)	1
OS-109	I.C. 74S109 (U13)	1
OO-154	I.C. 74154 (U22)	1
IC-558	I.C. NE558 (U28)	1
IC-741	I.C. 741N (U29)	1
IC-732	I.C. 2732 (U2)	1
IC-164	I.C. 4164 (U1,4,5,10,14,17,18,23)	8
IC-502	I.C. 6502 (U15)	1
IC-301	I.C. 65301 (U11)	1
IC-371	I.C. 65371 (U24)	1
IC-PAL	I.C. 16R8 (U9)	1
R4-47R	47 OHM 1/4W (R4,15,16,19)	4
R4-51R	51 OHM 1/4W (R18)	1
R4-68R	68 OHM 1/4W (R35,42)	2
R4-100	100 OHM 1/4W (R22-25,33,34,37)	7
R4-120	120 OHM 1/4W (R6-8,11)	4
R4-150	150 OHM 1/4W (R14)	1
R4-220	220 OHM 1/4W (R43)	1
R4-270	270 OHM 1/4W (R2,17)	2
R4-330	330 OHM 1/4W (R27)	1
R4-680	680 OHM 1/4W (R10)	1
R4-1K0	1K OHM 1/4W (R3,5,9,12,13,49,51,52)	8
R4-2K0	2K OHM 1/4W (R20)	1
R4-2K7	2.7K OHM 1/4W (R30)	1
R4-3K3	3.3K OHM 1/4W (R21,40,50)	3

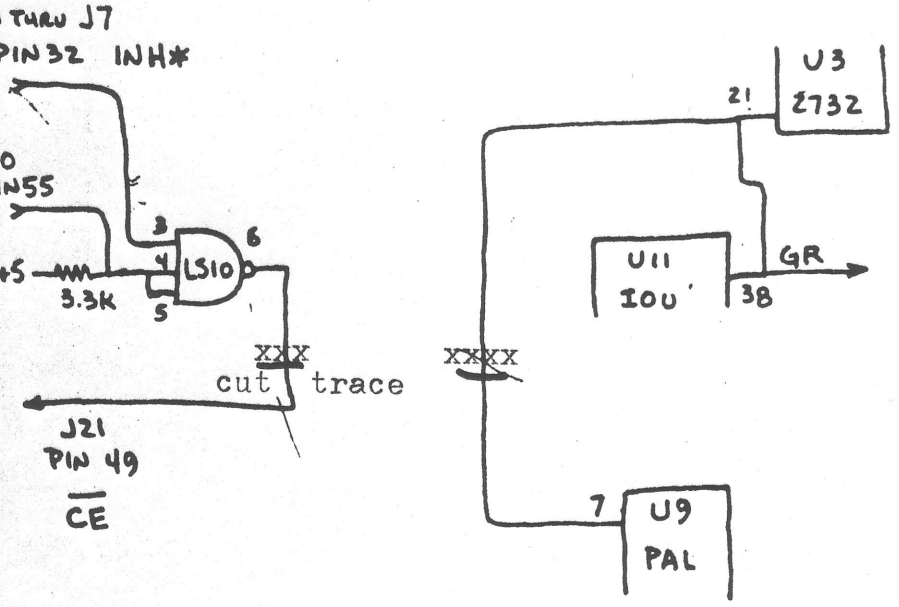
R4-5K6	5.6K OHM 1/4W (R29).....	1
R4-6K8	6.8K OHM 1/4W (R28,31).....	2
R4-12K	12K OHM 1/4W (R36,38,39,44-46, 48).....	7
R4-51K	51K OHM 1/4W (R41).....	1
R4-1MO	1M OHM 1/4W (R47).....	1
R2-91R	91 OHM 1/2W (R1).....	1
RS-1KO	1K RES SIP 10 PIN 9 RES (RP3).	1
RS-3K3	3.3K RES SIP 10 PIN (RP1,2)...	2
CP-470	47 pF CAP. (C62).....	1
CP-101	100pF CAP. (C63,79).....	2
CP-221	220pF CAP. (C6-8,31).....	4
CP-223	0.022uF CAP. (C69-71,73).....	4
CP-104	0.1uF CAP. (C9-30,32-58,60,61, 64-68,72,74-78,80)	63
CP-106	10uF 16V CAP. (C1-5,59).....	6
CV-50P	50 pF TRIM CAP. (VC1,2).....	2
ID-276	27uH INDUCTOR (L6).....	1
ID-XXX	XXXuH INDUCTOR (L1-5).....	5
TQ-904	2N3904 TRANSISTOR (Q3).....	1
TQ-906	2N3906 TRANSISTOR (Q1,2,4)....	3
TQ-A13	MPSA13 TRANSISTOR (Q5).....	1
CR-148	1N4148 DIODE (CR1,2).....	2
CY-143	14.31818 MHZ CRYSTAL (Y1).....	1
CN-60P	60 PIN CARD EDGE CON. (JO)....	1
CN-50P	50 PIN CARD EDGE CON (J1-7,21)	8
CN-9DF	9 'D'ST. FEMALE CON. (J8).....	1
CN-CAS	CASS. CONNECTOR (J9,10).....	2
CN-RCA	RCA TYPE VIDEO CON. (J11).....	1
CN-PS6	6 PIN POWER CON. (J21).....	1
HD-4PN	4 PIN HEADER (J13).....	1
HD-2PN	2 PIN HEADER (J18).....	1
SC-08P	8 PIN SOCKET (U29).....	1
SC-14P	14 PIN SOCKET (U8,12,21,25)...	4
SC-16P	16 PIN SOCKET (U1,4,5,7,10,13, 14,16,17,18,23, 26,28,J15,J17)	15
SC-20P	20 PIN SOCKET(U2,6,9,19,20,27)	6
SC-24P	24 PIN SOCKET (U3,22).....	2
SC-40P	40 PIN SOCKET (U11,15,24).....	3

Addendum

CEC IIe

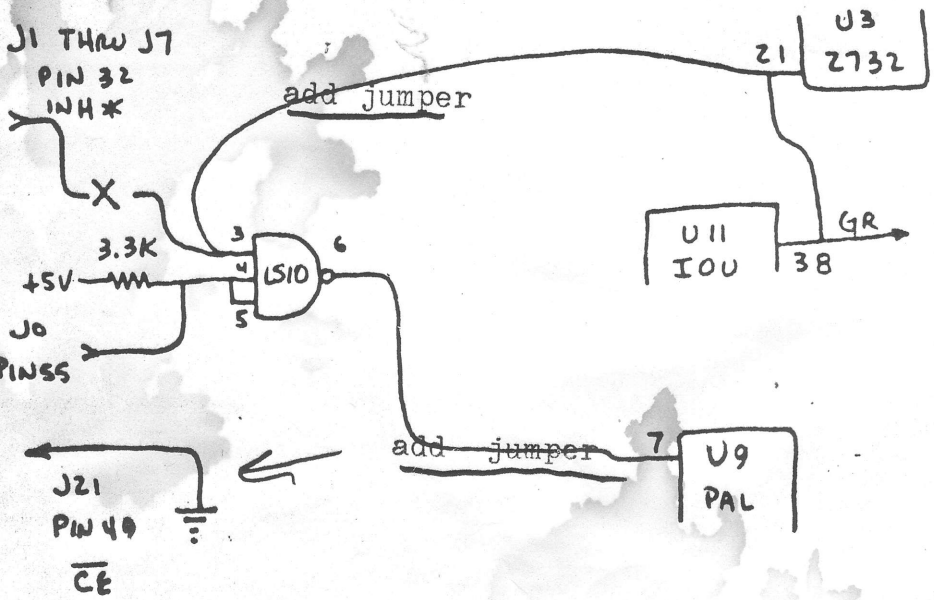
It has come to our attention that some motherboards are having a video problem.
The following changes to the board will correct these problems.

ORIGINAL CONNECTIONS

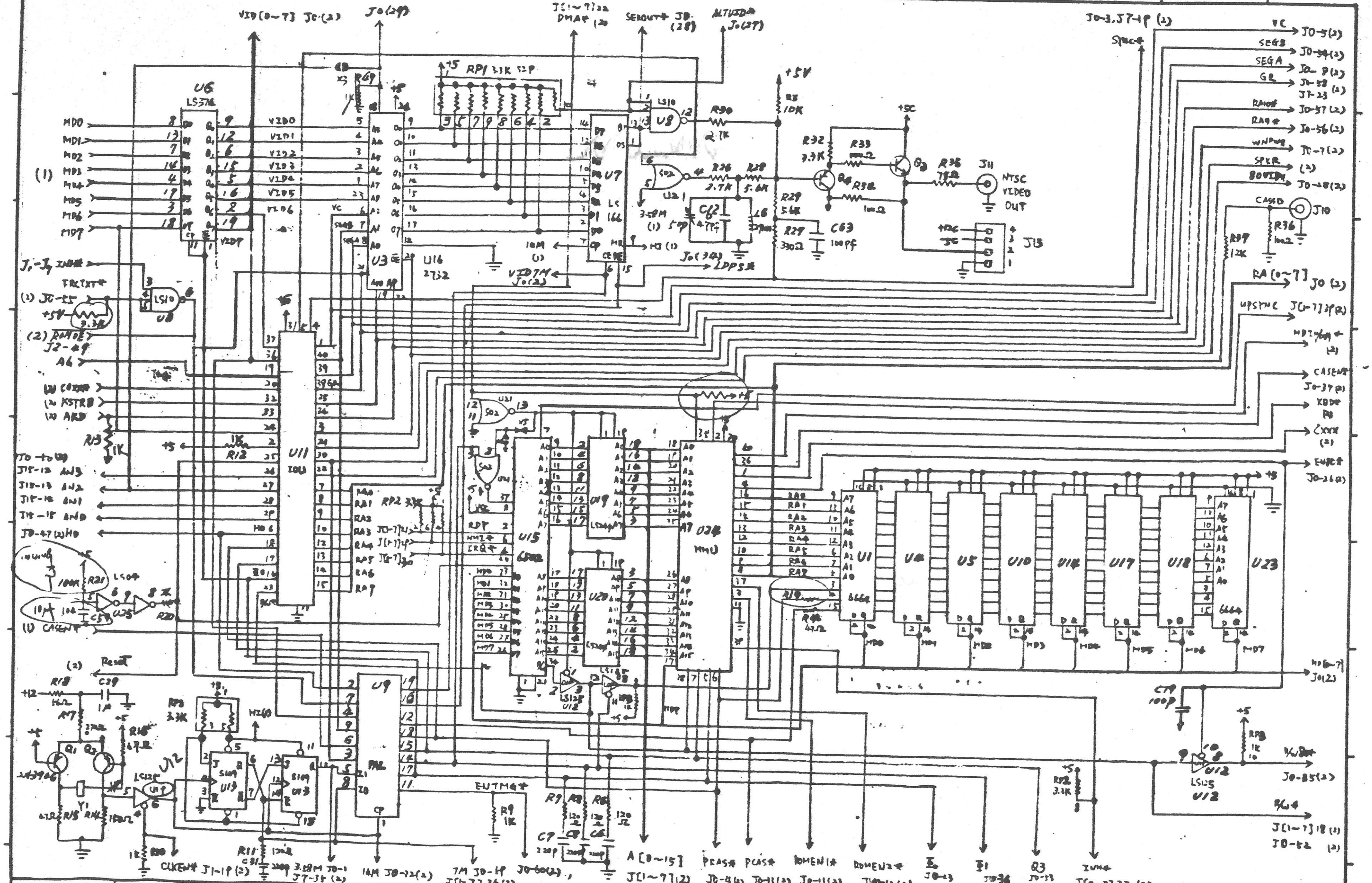


NOTE: LOGICAL INVERSION IS REQUIRED ON THE "GR" SIGNAL TO U9 PIN7 FOR TEXT & GRAPHICS TO WORK PROPERLY

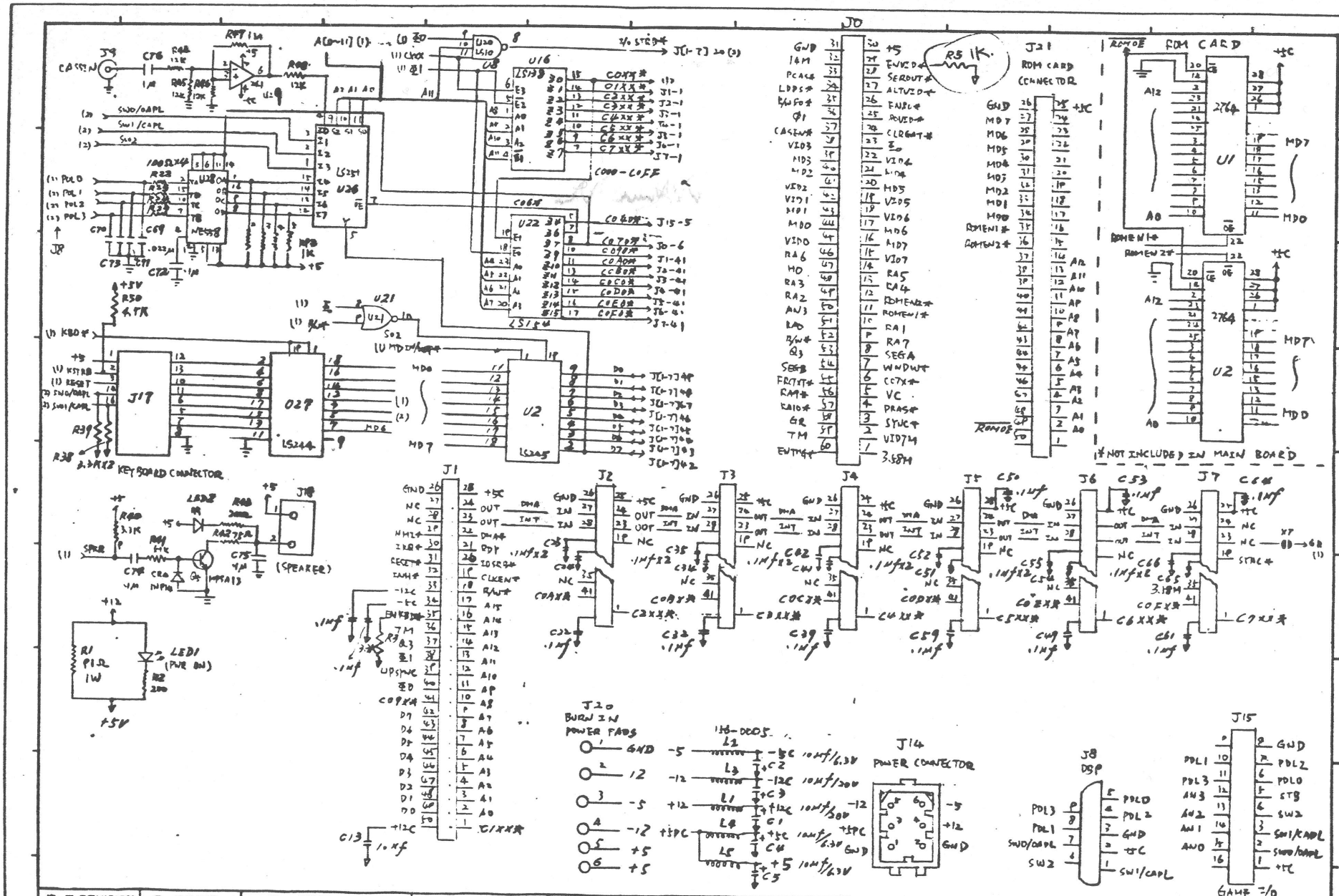
REQUIRED CONNECTIONS



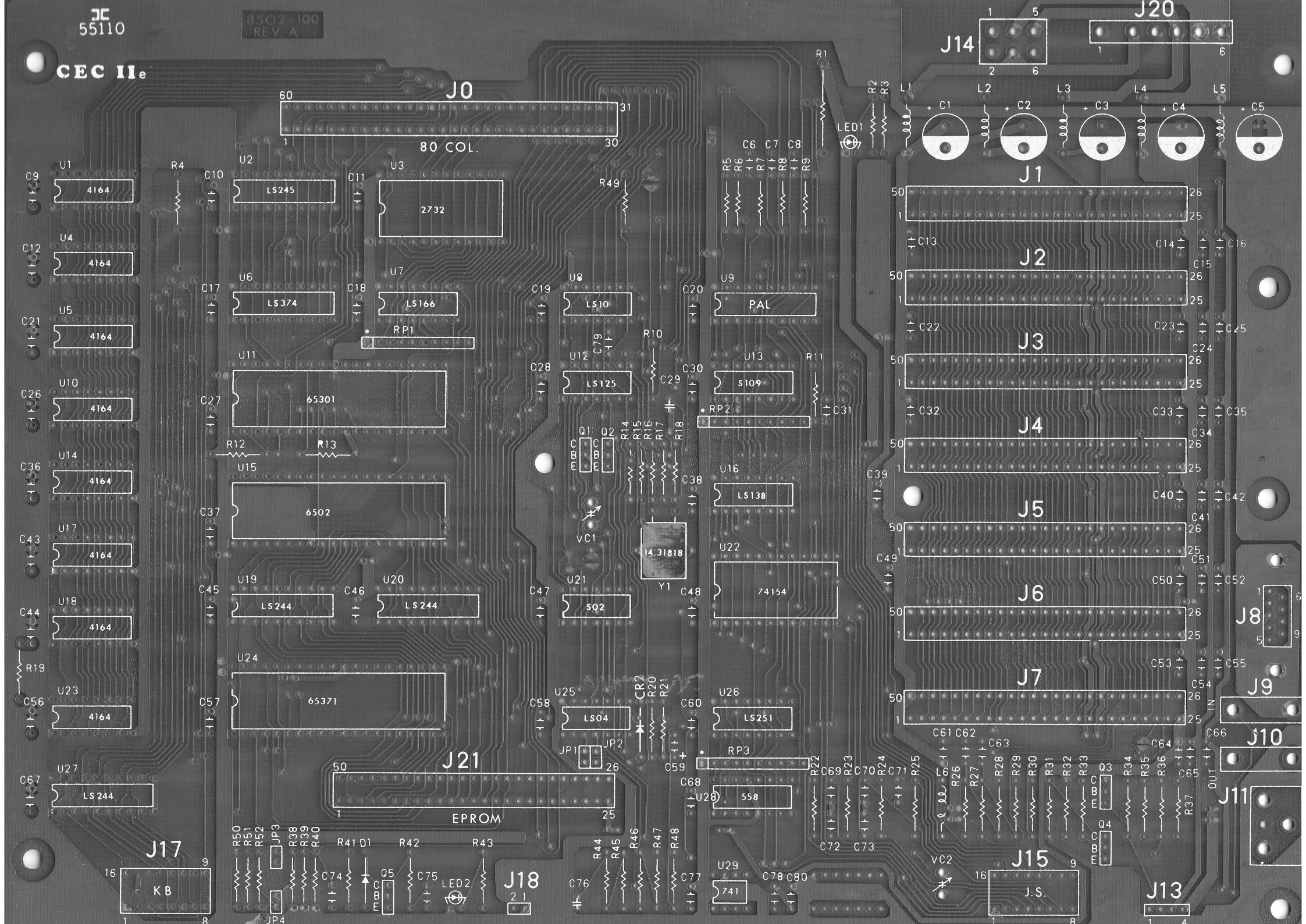
NOTE: THIS BRINGS CEC IIe INTO CONFORMANCE WITH APPLE™ IIe



修 正 REVISION	日 期 DATE	說 明 DESCRIPTION	核 准 APPROVAL BY	繪 圖 DRAWN BY	設 計 DESIGNED BY	比例尺 SCALE	圖 號 DRAWING NO	業務號 JOB NO	張 號 SHEET NO
				核 對 CHECKED BY	核 准 APPROVED BY	日 期 DATE			1-2



修正 REVISION	日期 DATE	說明 DESCRIPTION	核准 APPROVED BY	繪圖 DRAWN BY		設計 DESIGNED BY		比例尺 SCALE			圖號 DRAWING NO	業務號 JOB NO	張號 SHEET NO
				核對 CHECKED BY		核准 APPROVED BY		日期 DATE					2-2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EPROM
KB
J.S.
U1 4164
U2 LS245
U3 2732
U4 4164
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U6 LS374
U7 LS166
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U13 S109
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U25 LS04
U26 LS251
U27 LS244
U28 558
U29 741
RP1
RP2
RP3
Y1 14.31818
LED1
LED2
VC1
VC2
JP1
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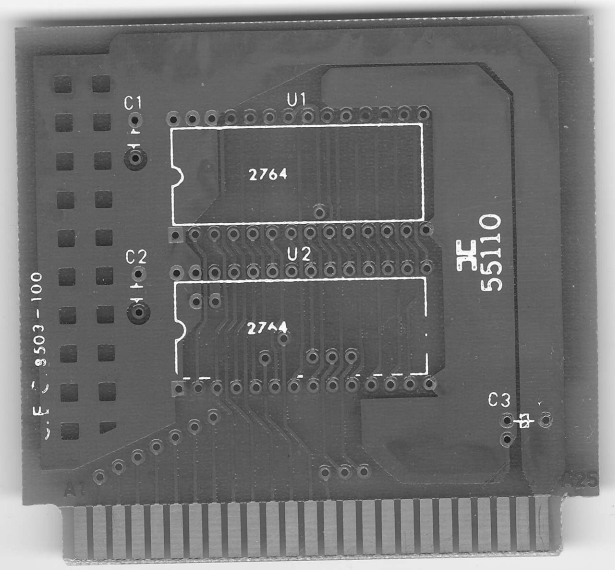
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